IN THE CLAIMS

1. [Currently Amended-Figure 3 embodiment] ~~An integrated circuit~~ A device ~~structure~~ comprising:

a plastic or glass or plastic laminated to glass substrate;

a layer of substrate insulation comprised of silicon dioxide or silicon nitride formed on said substrate using low-temperature, thin-film integrated circuit processing techniques performed using temperatures and materials which will not damage said substrate, said layer formed so as to have ~~having~~ a thickness, given the Young's Modulus and type of material of said layer of insulation and the Young's Modulus, thickness and type of material of said substrate, such that little or no differential strain between said ~~the~~ substrate and said layer of substrate insulation occurs at any temperature in the normal operating temperature range of said device; ~~integrated circuit;~~

an antenna conductor which is bonded onto, integrated onto or printed onto said layer of substrate insulation ~~substrate~~ and having two conductive pads or other conductive terminal areas where electrical connection to said antenna is capable of being made;

an antenna insulation layer formed over said antenna conductor using low-temperature, thin-film integrated circuit fabrication techniques using temperatures and materials which will not damage previously formed structures of said device, said antenna insulation layer formed so as to have vias or contact holes over said conductive terminal areas of said antenna conductor;

a layer of silicon deposited on said antenna insulation layer using thin-film, low-temperature integrated circuit processing techniques using temperatures

and materials which will not damage previously formed structures of said device;

an integrated circuit comprising an RFID tag or smart card transceiver and processor and memory ~~integrated circuit~~ integrated ~~on said substrate~~ in said layer of silicon using low-temperature, thin-film integrated circuit processing techniques carried out at temperatures and using materials which will not damage previously formed structures of said device and formed so as to have ~~RF~~ input/output terminals which are electrically coupled to said conductive terminal areas of said antenna.

2. [Currently Amended - Figure 1 embodiment] A ~~An integrated circuit~~ device ~~structure~~ comprising:

a plastic or glass or plastic laminated to glass substrate;

a layer of substrate insulation comprised of silicon dioxide or silicon nitride or a combination of silicon dioxide and silicon nitride formed on said substrate using low-temperature, thin-film integrated circuit processing techniques performed using temperatures and materials which will not damage said substrate, said layer of substrate insulation formed so as to have ~~having~~ a thickness, given the Young's Modulus and type of material of said substrate insulation layer o and the Young's Modulus, thickness and type of material of said substrate, such that little or no differential strain between said ~~the~~ substrate and said layer of substrate insulation occurs at any temperature in the normal operating temperature range of said device ~~integrated circuit~~;

a layer of silicon deposited on said layer of substrate insulation using thin-film, low-temperature integrated circuit processing techniques using temperatures and materials which will not damage previously formed structures

of said device;

an integrated circuit comprising an RFID tag or smart card transceiver having antenna contacts and a processor and a memory ~~integrated circuit~~ integrated into said layer of silicon using low-temperature, thin-film integrated circuit fabrication techniques performed using temperatures and materials which will not damage previously formed structures on said device, ~~on said substrate on top of said insulation layer of silicon dioxide or silicon nitride~~ said transceiver portion of said integrated circuit formed so as to have RF input/output terminals, ~~and having a layer of insulating material formed over said integrated circuit~~;

an integrated circuit insulating layer formed over said integrated circuit using low-temperature, thin-film integrated circuit fabrication techniques using temperatures and materials which will not damage previously formed structures of said device, and having contact holes formed therethrough to allow electrical connection to said RF input/output terminals of said transceiver;

an antenna conductor which is bonded onto, integrated onto or printed onto said integrated circuit insulating layer covering said transceiver ~~integrated circuit~~ so as to make electrical connection with said RF input/output terminals of said transceiver. ~~RF input/output terminals~~.

3. [Currently Amended] ~~An integrated circuit~~ A device ~~structure~~ comprising:

a first plastic or glass or plastic laminated to glass substrate;

a substrate insulation layer of silicon dioxide or silicon nitride formed on said substrate using integrated circuit processing techniques having temperatures and materials which will not damage said substrate, ~~having~~ said substrate insulation layer formed so as to have a thickness selected given the

Young's modulus of the material of said substrate insulation layer such that little or no differential strain between the substrate and said substrate insulation layer occurs at any temperature in the normal operating temperature range of said device; ~~integrated circuit;~~

an antenna conductor which is bonded onto, integrated onto or printed onto said substrate insulation layer and having two conductive pads or other conductive terminal areas where electrical connection to said antenna is capable of being made;

an RFID tag or smart card transceiver integrated circuit integrated using semiconductor processing techniques on a second plastic or glass substrate using flat panel display manufacturing equipment, said integrated circuit being cut from said second plastic or glass substrate and bonded or otherwise attached to said first plastic substrate and having RF input/output terminals; and

wires connected between said RF input/output terminals of said integrated circuit and said terminal areas of said antenna.

Please add a new claim 4 as follows:

4. A memory device comprising:

a plastic or glass or plastic laminated to glass substrate;

a layer of substrate insulation comprised of silicon dioxide or silicon nitride formed on said substrate using low-temperature, thin-film integrated circuit processing techniques performed using temperatures and materials which will not damage said substrate, said layer formed so as to have a thickness, given the Young's Modulus and type of material of said layer of insulation and the Young's Modulus, thickness and type of material of said substrate, such that little or no differential strain between said substrate and said layer of substrate insulation

occurs at any temperature in the normal operating temperature range of said device;

a layer of silicon deposited on said antenna insulation layer using thin-film, low-temperature integrated circuit processing techniques using temperatures and materials which will not damage previously formed structures of said device;

an EEPROM memory having a source, drain and channel region integrated in said layer of silicon and having a gate insulation layer formed over said channel region which is thin enough to allow tunnelling when programming voltages are applied, and having a gate, and having an intergate insulation layer formed over said gate, and having a control gate formed over said intergate insulation layer, all said structures forming said EEPROM memory formed using low-temperature, thin-film integrated circuit processing techniques carried out at temperatures and using materials which will not damage previously formed structures of said device;

an EEPROM insulation layer formed over said EEPROM memory using low-temperature, thin-film integrated circuit processing techniques carried out at temperatures and using materials which will not damage previously formed structures of said device; said insulation layer formed so as to have contact holes therein to allow electrical contact to said control gate and said source and drain regions of said EEPROM memory;

a contact metallization layer formed over said EEPROM insulation layer so as to make electrial contact with said control gate and said source and drain regions of said EEPROM memory.